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High-Speed, Low-Voltage, and Environmentally Stable Operation of Electrochemically Gated Zinc Oxide Nanowire Field-Effect Transistors

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Single-crystal, 1D nanostructures are well known for their high mobility electronic transport properties. Oxide-nanowire field-effect transistors (FETs) offer both high optical transparency and large mechanical conformability which are essential for flexible and transparent display applications. Whereas the "on-currents" achieved with nanowire channel transistors are already sufficient to drive active matrix organic light emitting diode (AMOLED) displays; it is shown here that incorporation of electrochemical-gating (EG) to nanowire electronics reduces the operation voltage to ≤2 V. This opens up new possibilities of realizing flexible, portable, transparent displays that are powered by thin film batteries. A composite solid polymer electrolyte (CSPE) is used to obtain all-solid-state FETs with outstanding performance; the field-effect mobility, on/off current ratio, transconductance, and subthreshold slope of a typical ZnO single-nanowire transistor are 62 cm^2/Vs, 10^7, 155 μS/μm and 115 mV/dec, respectively. Practical use of such electrochemically-gated field-effect transistor (EG FET) devices is supported by their long-term stability in air. Moreover, due to the good conductivity (≈10^{-2} S/cm) of the CSPE, sufficiently high switching speed of such EG FETs is attainable; a cut-off frequency in excess of 100 kHz is measured for in-plane FETs with large gate-channel distance of >10 μm. Consequently, operation speeds above MHz can be envisaged for top-gate transistor geometries with insulator thicknesses of a few hundreds of nanometers. The solid polymer electrolyte developed in this study has great potential in future device fabrication using all-solution processed and high throughput techniques.

1. Introduction

Research efforts on transparent and flexible field-effect devices as fundamental building blocks of many modern electronic applications have gained tremendous momentum over the last decade. After commercialization of the flat-panel displays, it has been possible to foresee the emergence of a brand new market for flexible and transparent displays in the future. Consequently, a lot of research efforts have been concentrated on transparent oxide thin film transistors (TFTs) which have shown excellent electrical characteristics and large field-effect mobility values,[1–5] as opposed to mechanical conformability issues which have not yet been completely overcome. In this regard, high performance metal oxide nanowire transistors are one of the choices fulfilling all the requirements that are essential for transparent and bendable displays.[6–11] Although the successful and efficient alignment methods for these one-dimensional nanostructures still needs further research attentions, the review by Fan et al.[12] has exquisitely summarized several experimental procedures describing controlled positioning or alignment techniques for nanowires or nanorods.

Among others (which are equally good in terms of FET performance), zinc oxide nanowire FETs have been most extensively[13–17] studied as ZnO simultaneously meets many requirements: it is environmentally friendly,[18] nontoxic, low-cost,[19] and can be prepared on a large scale by following inexpensive synthesis routes.[20] Although the flexible nanowire FETs have been studied by many other groups, we believe that in order to exploit all potential areas of application, such as AMOLED display drivers, large-area see-through sensors, coverage of various curved surfaces

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(e.g., car interiors and sunroofs etc.),[21–24] it would be of great interest to try out battery compatible, portable devices. This, in turn, limits the drive voltages to only a few volts. In this context, low operating voltage oxide nanowire FETs have been scarcely reported in the past, the majority of which have either used low-leakage, high-k inorganic oxide gate dielectrics, such as Al_2O_3 and HfO_2[25–27] or organic self-assembled ultrathin nano-dielectrics (SAND).[28–32] Although the ultrathin monolayer or multilayer organic nano-dielectrics show excellent insulating properties and quite outstanding device performances,[33–34] the preparation of the densely-packed SAND layers is generally very time consuming and preferential positioning of the SAND layers with solution processing is quite unlikely as they usually tend to cover the complete substrate.

In this regard, we introduce a new approach by incorporating composite solid polymer electrolytes (CSPE) as the gate-insulator to control the current through ZnO single-nanowire transistors which simultaneously enables low voltage operation, ensures mechanical flexibility and high optical transparency. Additionally, unlike ionic liquids[35] which are quite extensively studied as gate-insulators recently, the CSPE is found to be extremely stable in ambient conditions and the CSPE-gated nanowire FETs show long-term stability in air. In order to ensure electrostatic doping and to avoid the presence of any chemical reactions at the nanowire/CSPE interface, a careful selection of the supporting electrolyte and a judicious control of the applied gate potential are exercised. In addition, it is shown that the electrolytic insulator can easily be ink-jet printed, bringing about an opportunity to realize high-throughput, all-solution-processed nanowire channel FETs, given that the nanowires can be aligned with sufficient accuracy.[12] It is also important to note that owing to large conductivity of the CSPE used in this study, it is possible to attain over MHz switching frequency using such EG FETs, which is quite sufficient for driving limited-pixel AMOLED displays. The high transparency of the CSPE reported in this work, may also be utilized in order to build nanowire FET-based, high performance optical and UV sensors.[36,37]

2. Results and Discussion

2.1. Synthesis and Structural Characterization of ZnO Nanowires

Single-crystalline, phase-pure ZnO nanowires have been prepared following the vapor-liquid-solid mechanism (VLS).[38] Schematic representation of the experimental set up is shown in **Figure 1**. A gold film prepared with molecular beam epitaxy (MBE) with a nominal film thickness of 0.5 nm has been used as the catalyst. Firstly, the substrates (Si wafers) with the gold catalysts are loaded into the reactor; next, the reactor is moved inside a tube furnace which has been preheated to 910 °C. X-ray diffraction (XRD) measurements are performed on as-grown ZnO nanowires (**Figure 2**a). The first three diffraction peaks can be easily identified as $(2\bar{1}\bar{1}0)$, (0002), and $(11\bar{2}0)$ reflections, when compared to the line spectrum of bulk polycrystalline ZnO which possess a wurtzite hexagonal structure (ICSD No. 031060). The absence of any spurious diffraction peaks

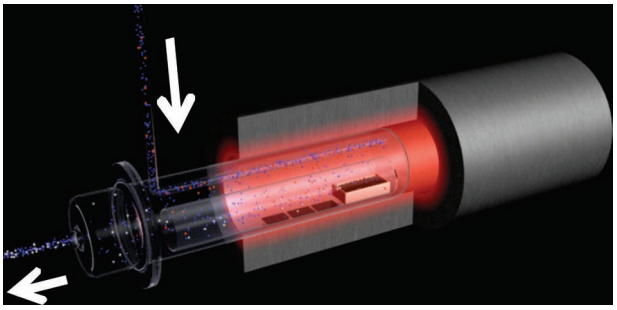

Figure 1. Schematic presentation of the quartz tube (reactor) used for the nanowire growth.

indicates the formation of pure ZnO nanowires. The reflection which belongs to the single crystalline Si substrate is marked in red. Energy dispersive X-ray spectroscopy (EDX) (Figure S1, Supporting Information) has also been performed as an additional characterization tool to confirm the phase purity. Scanning electron microscopy (SEM) images (a characteristic image is shown in Figure 2b) acquired on the as-grown samples show ZnO nanowires and gold catalysts on top of each nanowire confirming the VLS growth mechanism. The average nanowire

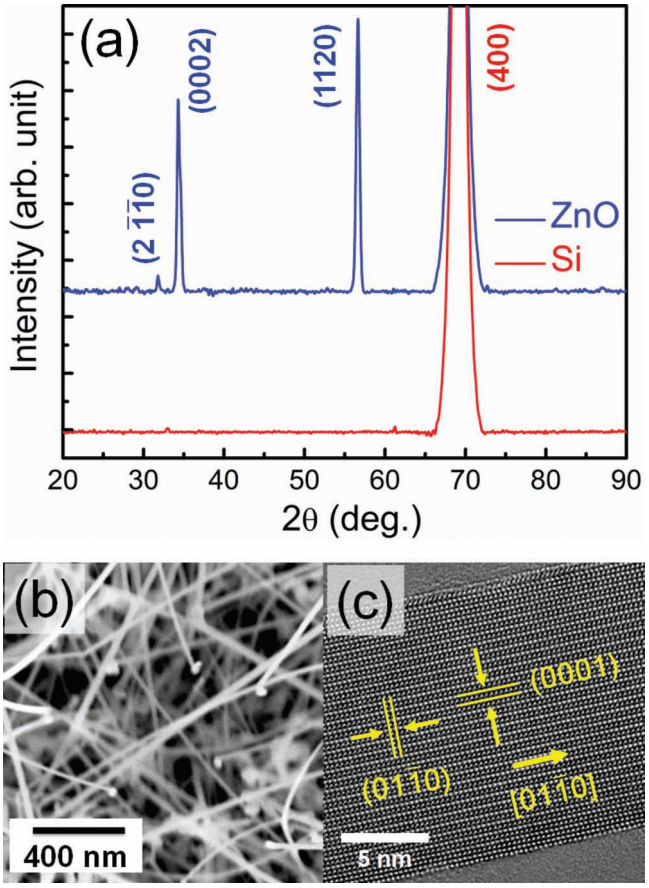

Figure 2. a) XRD pattern of the ZnO nanowires; b) SEM image of a bundle of ZnO nanowires on the as-grown silicon wafer; c) HRTEM of an individual ZnO nanowire showing the $[01\bar{1}0]$ growth direction of the hexagonal wurtzite lattice of ZnO.

diameter is determined from SEM images and is found to be ca. 23 nm (Figure S2, Supporting Information). Figure 2c shows a high-resolution transmission electron microscopy (HRTEM) image of a single nanowire which confirms their single crystallinity. The fast Fourier transform (FFT) of the HRTEM images (e.g., Figure S3b, Supporting Information) show that the growth direction of the nanowires, in most cases, is perpendicular to the $(01\bar{1}0)$ planes which translate to $[01\bar{1}0]$ growth direction in hexagonal wurtzite lattice structure of ZnO.

2.2. Mechanical Conformability

In many occasions during the TEM examinations, the ZnO nanowires have been found to be remarkably bent as shown in **Figure 3**a (the bending radius, $r_b < 6$ µm in this particular case); the resulting strain is attributed mainly to elastic lattice distortions, because no plastic distortion ε_{xx} is observed in any of the HRTEM images that are taken (Figure 3b) along the curvature of the bent nanowires. In order to further examine the elasticity and mechanical robustness of these super-flexible nanowires, the strain tensor component, ε_{xx}, (Figure 3c) and rigid-body rotation (Figure 3d) of the bent segment of the nanowire (Figure 3b) has been calculated using the geometric phase analysis (GPA).[39] Figure 3e shows the strain profile (strain tensor component ε_{xx}) measured across the bent segment of the nanowire which is indicated by the black rectangle in Figure 3c. Compressive and tensile strain is found in the lower and the upper part of the nanowire, respectively, and a total strain difference of 2.5% is observed. Additionally, a profile of the rigid-body rotation has been measured along the length the nanowire (as indicated by the rectangular box in Figure 3d), which shows a rotational gradient of the nanowire axis of about 2.5° from one end to the other, already within ca. 30 nm of length segment. Therefore, it may be concluded from the GPA analysis that the nanowires can be moderately bent without causing any plastic deformations, such as dislocations or other defects; this result strongly suggests that such nanowire channels should be able to bend elastically and would perform well even when an ultraflexibility is on demand.

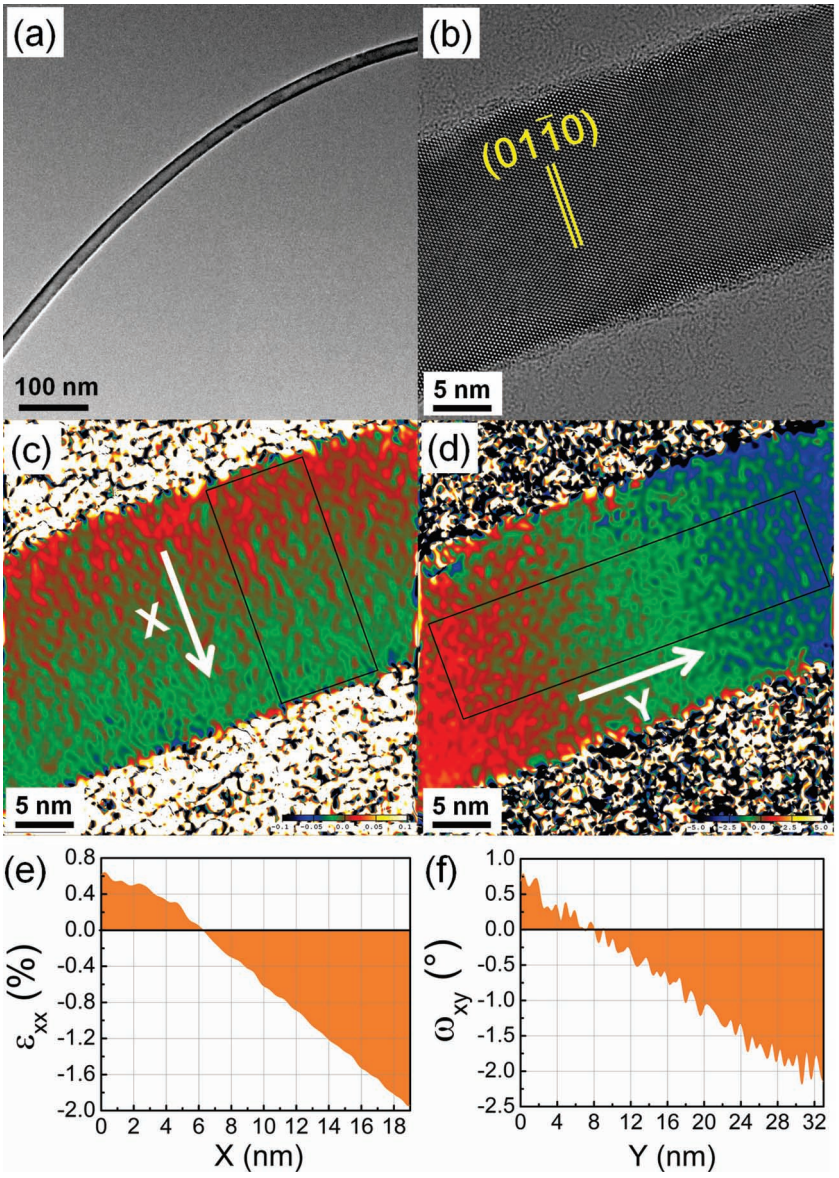

Figure 3. a) TEM image of a typical bent ZnO nanowire; b) HRTEM image along the curved part of the nanowire; c) strain map showing the strain tensor component ε_{xx}; d) rotation map showing the rigid-body rotation (strain tensor component ω_{xy}); e) strain profile of ε_{xx} measured across the nanowire and averaged over the width of the rectangular box as indicated in (c); f) rigid-body rotation measured along the nanowire and averaged over the width of the box as indicated in (d).

2.3. Preparation and Static Electrical Characterization of Nanowire-Channel EG FETs

To prepare single nanowire channel field-effect transistors, the as-grown nanowires are transferred from the growth substrate (donor substrate) to a fresh thermally oxidized silicon-wafer with 200-nm silicon oxide (receiver substrate). The passive structures of FETs are designed using the e-beam lithography technique and Sn-doped indium oxide (ITO) electrodes are sputtered onto the lithographically defined structures to realize the FET devices. The complete process is shown schematically in **Figure 4**a–e. For simplicity all the transistors reported in this study are prepared as in-plane FETs, as shown in Figure 4e. As already mentioned, a composite solid polymer electrolyte which is composed of a synthetic polymer (polyvinyl alcohol, PVA), a plasticizer (propylene carbonate, PC), a solvent (dimethyl sulfoxide, DMSO) and a supporting electrolyte (lithium

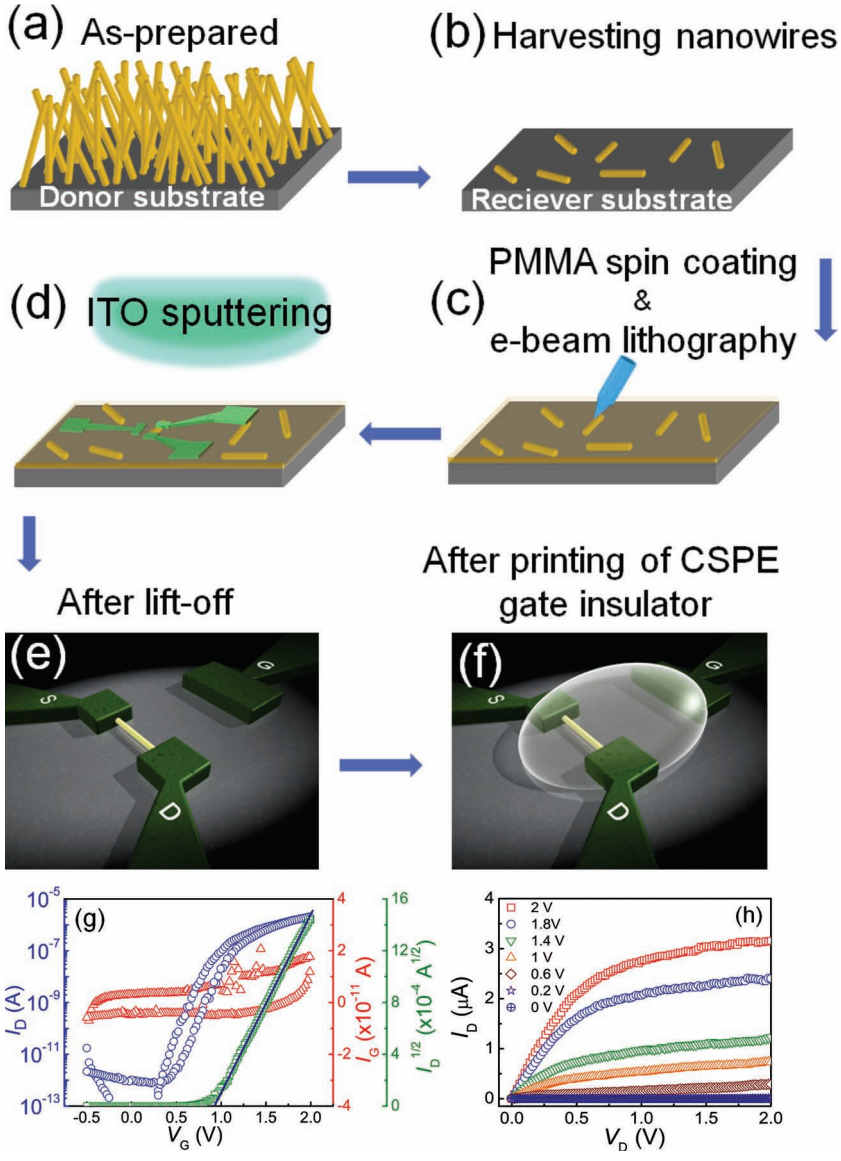

Figure 4. Schematic representation of the device preparations steps: a) as-prepared nanowires on a donor substrate; b) the nanowires are transferred to the receiver substrate by simple physical contact method; c) spin coating of PMMA as the positive resist to perform e-beam lithography; d) after the development, the ITO electrodes are deposited by RF magnetron sputtering; e) the device geometry after the lift-off; f) the view of the EG FET device after ink-jet printing of the CSPE; g) transfer characteristics of a typical ZnO nanowire channel EG FET device, the applied drain voltage is V_D = 0.5 V, the blue circle, the green square and the red triangle symbols represent the drain current, the square root of the drain current and the gate current, respectively. The threshold voltage (V_T) is calculated to be 0.93 V by extrapolating the linear part of the $I_D^{1/2}$; h) drain current-drain voltage (I_D–V_D) output characteristics of the device, while the gate voltage (V_G) is varied between 0 to 2 V.

perchlorate, $LiClO_4$) has been used as the gate insulator. The electrolyte is usually ink-jet printed in the liquid form and is eventually solidified with evaporation of the excess solvents. Because of the high boiling point of the DMSO and PC, their room temperature vapor pressures are considerably low. Consequently, a significant amount of solvent remains trapped inside the polymeric network in the dried form of the electrolyte, which in turn results in a high value of conductivity of the solid polymer electrolyte of around 10^{-2} S/cm.[40] The polymer electrolyte is printed with a Dimatix ink-jet printer, in a way to cover the nanowire channel completely and the in-plane gate electrode partially, as shown in Figure 4f and then allowed to dry at room temperature to obtain an all-solid-state device. The transistor characteristics of a typical nanowire EG FET device are shown in Figure 4g,h. The transfer curve, which is shown in Figure 4g, illustrates the behavior of a normally-off electron conducting (*n*-type) metal oxide semiconductor field-effect transistor (MOSFET). At zero gate bias, the off-current is less than a picoampere, however, owing to the high double-layer capacitance of the electrolyte, a substantial on-current of several microamperes can be driven even though the applied gate voltage is always limited to ≤2 V. On the other hand, this constraint in applied gate voltage has helped to restrict any faradaic currents from flowing through the electrochemical capacitor. This fact is further supported by the excellent insulating property of the electrolyte with only an ultralow and ideal capacitor-like constant gate currents (I_G) of around 10 pA (Figure 4g). The (channel width) specific transconductance (g_m) of the device with 18-nm diameter of the nanowire channel is found to be 155 μS/μm. The subthreshold slope (S), which is defined as the gate voltage that is necessary to alter the drain current by one order of magnitude, i.e., $S = dV_G/d(\log I_D)$, is found to be only 115 mV/decade; whereas 60 mV/decade is the theoretical limit. The small subthreshold slope ensures small voltage requirement to switch the transistor to the on-state. The threshold voltage (V_T) of all the measured FETs has always been positive while the V_T of the device presented in Figure 4g is calculated to be 0.93 V. This indicates an accumulation-mode operation of the ZnO nanowire channel transistors which, in combination with an ultralow value of the off-current, inspires possibilities of low-power logic operations. The large value of on-currents, on-off ratio, transconductance, and a small subthreshold slope in combination with absolutely negligible leakage currents are either comparable or superior to the best ZnO nanowire-based FETs that are reported in the literature.[8,13,30,31]

The other important figure of merit, field-effect mobility (μ_{FET}) of a transistor at its saturation regime ($V_D > V_G - V_T$) can be calculated by the following equation:[41]

$$\mu_{FET} = \frac{I_D \times 2L}{W \times C_{DL} \times (V_G - V_T)^2} \quad (1)$$

where L, the channel length (940 nm for the transistor shown in Figure 4); W, the channel width; I_D, the saturated drain current at the gate voltage V_G and V_T, the threshold voltage. For the presented EG FET device, the specific capacitance of the dielectric (C) in Equation (1) is considered to be equal to the double layer capacitance (C_{DL}) of the electrochemical capacitor; C_{DL} has been calculated with the cylindrical capacitor model which is composed of the nanowire and is surrounded by the solid polymer electrolyte:

$$C_{DL} = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln\left(1+\frac{l}{r}\right)} \quad (2)$$

where, ε_0, the permittivity of the free space, ε_r, the dielectric constant of the electrolyte solvent, r, the radius of the nanowire (9 nm for the device shown in Figure 4) and l, the dielectric thickness of the electric double layer (EDL) which can be considered to be 1 nm unless for an extremely diluted electrolyte which is definitely not the case over here.[42–44] The dielectric constant of the solvent of the electrolyte is taken to be 5, because it has been shown earlier in the literature that regardless of the bulk dielectric constant, at the vicinity of EDL, ε_r reduces to 5.[45,46] This has also been experimentally corroborated by demonstrating similar specific charge and hence capacitance for electrolytes with propylene carbonate, PC (ε_r = 65) and ethyl acetate, EA (ε_r = 6)[47] as solvents which possess completely different relative dielectric constants (Figure S4, Supporting Information). Therefore, using Equation (1) and Equation (2), it is possible to calculate the field-effect mobility of the present FET to be 61.7 cm^2/Vs. However, a maximum value of 98 cm^2/Vs for the field-effect mobility has been obtained for another device demonstrating that further increase of μ_{FET} can be achieved by process optimizations. The on/off ratio, saturated on-current, threshold voltage and field-effect mobility of 10 individual devices are summarized in Figure S5a,b (Supporting Information).

Figure 4h shows drain current-drain voltage characteristic of the ZnO EG FET, where the gate voltage (V_G) is varied between 0 to 2 V and the drain voltage is swept from 0 to 1.5 V. The output characteristic reveals quite decent current saturation at high V_D and an excellent linear behavior at low V_D indicating low resistance of the ohmic contacts formed between the ZnO nanowire and the ITO source/drain electrodes. The transistor already shows a high saturation current (≈3 μA) at values V_D = 0.5 V and V_G = 2 V indicating that the EG FETs are quite suitable for ultralow-voltage applications and are compatible with thin film batteries.

The same nanowire transistor as shown in Figure 4 (channel length = 940 nm and nanowire diameter = 18 nm) has also been used to build a rectifying diode and a simple MOS inverter (NOT logic gate), respectively. The electrical characteristics are shown in **Figure 5**. The rectifying diode is built by simply shorting the drain and gate electrodes and using the two terminals (the source electrode and shorted gate-drain electrode) as the terminals of a p-n junction diode (as shown in the inset of Figure 5a). The rectification ratio has always been observed more than three orders of magnitude; for example, the rectification ratio of 6.6 × 10^3 and 3.4 × 10^3 is observed for an input voltage of ±1.8 V and ±2 V, respectively. In addition, the threshold voltage of the transistor can again be corroborated by this diode configuration, with a linear fit of the forward biased diode response, as shown in Figure 5a, which interestingly results in a completely identical value of V_T = 0.934 V. The simple MOS inverter (NOT logic gate), on the other hand, has been fabricated with a constant external load resistor (R_L = 10 MΩ) as shown in Figure 5b, inset. The voltage transfer characteristic (VTC) is recorded for the supply voltage (V_D) of 1 to 2 V with every 0.2 V increment and the input voltage (V_G of the transistor) is swept from 0 to $V_G = V_D$. The resulting output voltage variation is shown in Figure 5b. The sharp inverter response to output switching has been clearly observed, which corresponds to gain values (dV_{out}/dV_{in}) of around 10, considerably large for an unipolar single-transistor NMOS inverter (Figure 5b). The purpose of demonstrating the diode and the single-transistor inverters has been to show that (although not with outstanding performances) simple logic operations are also possible with these NMOS EG FETs even when an equally good performance *p*-type MOSFET (PMOS) is not available.

2.4. Environmental Stability

Furthermore, it is of large importance to note that the composite solid polymer electrolyte used in the present study is extremely stable in ambient conditions. Figure S6 (Supporting Information) clearly shows that an electrochemical capacitor consisting of ITO electrodes and the CSPE retains 97% of its initial charge/capacitance after one month exposure to air. Air stability and long-term reproducibility of the EG FETs on the other hand are shown in **Figure 6**, illustrating four different electrochemically-gated ZnO nanowire transistors, whose transfer curves are measured at as-prepared condition and after twenty days in air. As a noticeable observation, the threshold voltage is seen to alter by a small amount with a maximum value of around 200 mV; however, there has not been any clear trend or preferred direction of this threshold voltage shift; hence it may not be related to certain physical effects in the nanowire FETs. On the other hand, no significant increase in hysteresis has been observed, in fact, in some cases the hysteresis is found to decrease with time. Additionally, as a general trend for all the measured devices, a small decrease in the gate leakage (may relate to further drying of the electrolyte) and a 2–3 fold increase in saturated gate current ($I_{D,sat}$) is recorded, which signifies even an increase in μ_{FET} is possible after several weeks of exposure to air.

2.5. Dynamic Electrical Characterization

Next, we discuss the most significant findings of the present study. The commonly encountered concern for the electrochemically-gated FETs relates to their switching speed. It is often argued that although devices with large mobility can be realized, however, they are usually of limited importance as the speed of EG FETs are actually governed by the ionic conductivity in the electrolyte.[48] This argument is of course partially true and especially valid for FETs with such high μ_{FET} as presented in this work, however, our recent studies involving the charging time of the electrochemical capacitors shows that

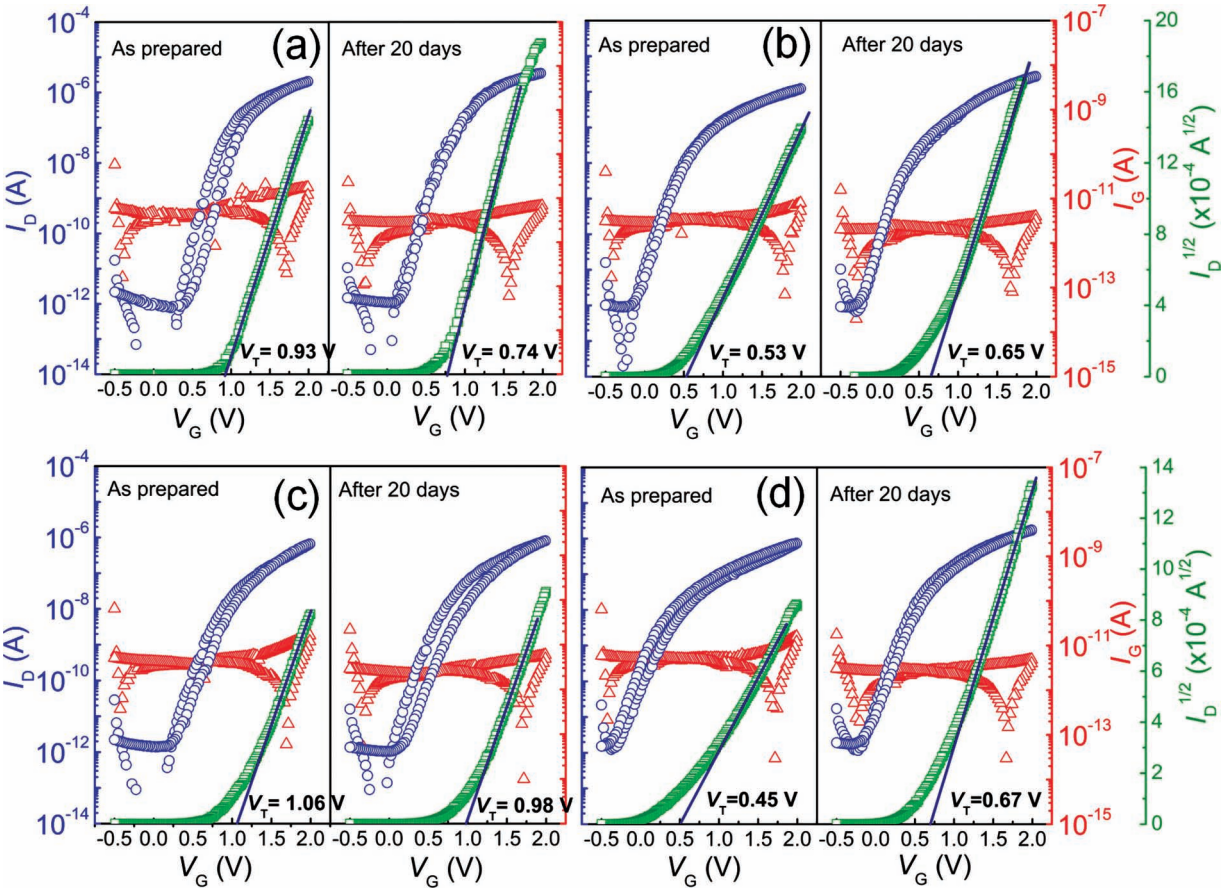

Figure 5. a) Electrical characterization of a diode fabricated by shorting the gate and the drain electrodes (as shown in inset); b) the voltage transfer characteristics and signal gain (dV_{out}/dV_{in}) of a typical inverter logic gate based on a CSPE-gated ZnO nanowire FET and a load resistor of $R_L = 10$ MΩ, under different V_D and input voltage (from 1–2 V with every 0.2 V increment); the inset shows the circuit design of the inverter.

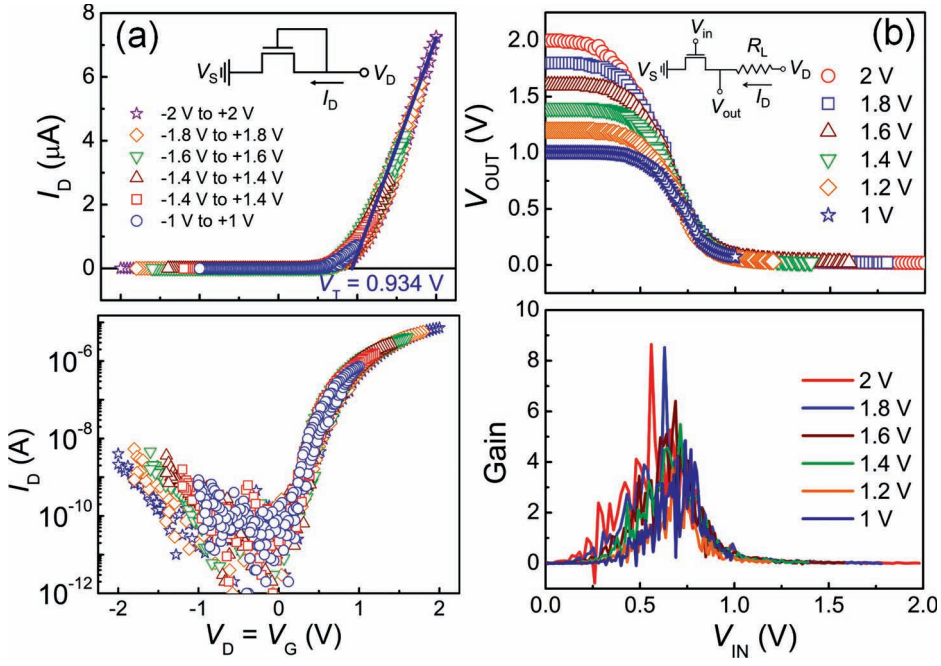

Figure 6. a–d) Transfer curves of randomly selected, four individual EG FET devices measured immediately after device fabrication and after 20 days in air, show long-term stability of the nanowire channel EG FETs and especially excellent stability of the CSPE in under ambient conditions.

for CSPE with a conductivity of 10^{-2} S/cm, attaining over MHz cut-off frequency may not be a problem for FETs with top-gate geometry and electrolyte thickness of several hundreds of nanometers.[40] Here, we show the experimental validity of the frequency dependent effective capacitance calculations which was presented earlier.[40] The time-resolved (transient) FET switching is performed with a zinc oxide EG FET where the source electrode is grounded, a constant potential of 2 V is applied to the drain and the potential at the gate is pulsed between −1 V to 2 V. Correction for the capacitive current from the passive structures has been made by subtracting the drain current recorded for zero drain voltage. The results are plotted in **Figure 7**a,b where Figure 7a shows the variation in the gate potential and Figure 7b illustrates the resultant drain current switching. An exponential fitting of the *rise* and the *fall* currents give the characteristic relaxation rise (τ_1) and fall (τ_2) times which are 9.5 and 0.88 μs, respectively. A larger rise time compared to the fall time has been reported earlier, and it has always been observed that electrochemical charging takes considerably longer period than discharging.[49,50] Taking inverse of the charging time we obtain the cut-off (f_T) frequency of the device, which is found to be greater than 100 kHz. While this value of cut-off frequency is already much larger than the other EG FET devices reported in the literature,[49,51–55] it is further important to note that the zinc oxide EG FET measured here being an in-plane transistor with a channel-gate distance larger than 10 μm, leaves a large scope for further improvement in speed and an increase in f_T beyond MHz regime just by a reduction in the gate-channel distance which can be easily achieved with a top-gate geometry. This is simply because of the fact that the electrochemical capacitors are *RC* circuits; and hence the relaxation time varies linearly with a decrease in the electrolyte resistance (*R*) which on the other hand scales with inter-electrode (i.e., gate-channel) distances.[42]

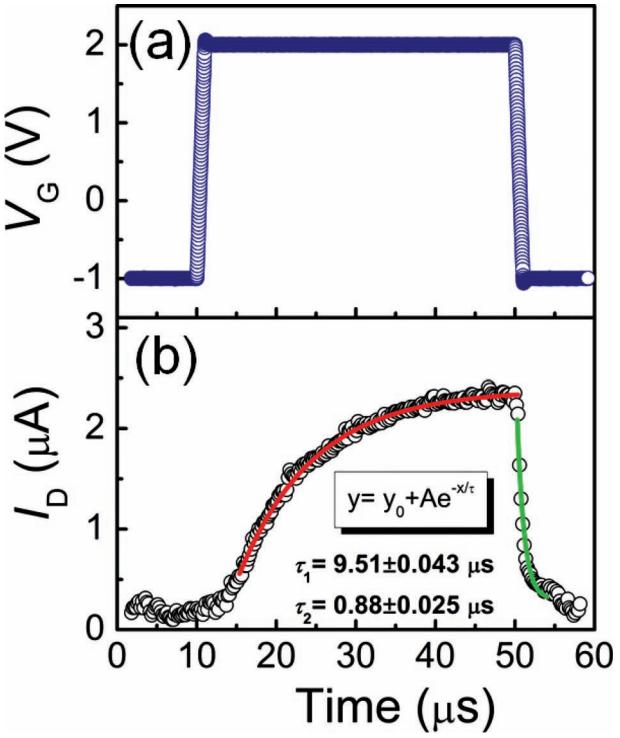

Figure 7. Time-transient measurement showing the switching speed of a single zinc oxide nanowire EG FET device; a) the gate voltage V_G is pulsed from −1 to 2 V, b) the corresponding response of the drain current (I_D) is recorded and both is plotted with respect to elapsed time, the rise and fall segments of the drain currents are separately fitted with exponential decay equations in order to obtain the charging (rise) and discharging (fall) time, respectively.

Nanowire channel EG FETs which are operating at low voltages and at high-speed is demonstrated. For applications using flexible substrates, the flexibility or bendability may not be a real concern with these devices as the nanowires are shown to possess high elasticity (as demonstrated in Figure 3). In addition to the nanowire channel and sputtered passive structures (ITO), the CSPE employed in this study also exhibits a high optical transparency as shown in Figure S8 (Supporting Information). Therefore, one may be optimistic enough to foresee flexible and portable AMOLED displays which are driven by the type of nanowire channel EG FETs, as presented in this study

3. Conclusions

We have presented electrochemically-gated field-effect transistors with the transistor channel being composed of single-crystalline high-mobility zinc oxide nanowires. The devices have been prepared on commercial silicon wafers; however, owing to the low processing temperatures, they should be compatible to inexpensive and flexible substrates, such as polymers, cellulose etc. It is shown that the EG FET devices show excellent transistor characteristics and can be operated with drive voltages as low as 2 V or less. It is further demonstrated that the electrochemical gating approach is not a real limitation to the switching speed of the device, as it is found that the frequency is in the range of 100 kHz is already achievable with an in-plane transistor geometry, which may be further increased to the MHz range by changing to a top-gate architecture. Unlike the ionic liquids which are frequently employed in other research works, the CSPE examined and utilized in this work is found to be stable under ambient conditions and the EG FETs have shown no noticeable degradation after an exposure of 3–4 weeks in air. Therefore, in summary, the presented device type can be extremely suitable to drive battery compatible flexible OLED displays provided a controlled and inexpensive alignment of nanowires at preferred positions is achieved. Furthermore, the all-solid-state EG FET device presented in this study is obviously much faster than any electrochemically-gated transistor reported earlier in the literature and therefore may pave a way to hitherto uncharted applications involving EG FETs.

4. Experimental Section

Substrate Preparation: Thermally oxidized silicon wafers were used (as-received) as the nanowire growth substrates; gold thin film of nominal thickness of 0.5 nm was grown using molecular beam epitaxy

(MBE). Next, the substrates were annealed at 500 °C in order to obtain spherical gold nanoparticles to be used as the catalysts for the nanowire growth.

Nanowire Fabrication: In this report, the ZnO nanowires were synthesized via a catalyst-mediated vapor-liquid solid (VLS) process. In general, the vapor-phase epitaxial growth technique requires a chamber, which sometimes also referred as a reactor. A quartz tube of a horizontal tube furnace is used as the reactor in this work where the carrier gas was introduced at the hot end of the tube (as shown in Figure 1) and was pumped out from the cold end. A one-end closed, comparatively thinner second tube, with about one-fourth of the reactor-tube diameter, was placed inside the reactor with the open end facing the cold end of the furnace. In this experimental setup, the source materials and the Si substrates were placed inside the thinner tube. A thoroughly ball-milled mixture of ZnO (99.999% purity, Sigma Aldrich) and graphite powder (99.9% purity, Chempur) with a weight ratio of 3:1 was placed inside an alumina crucible at the closed end of the thinner tube, i.e., at the higher temperature end. Au catalyst-coated silicon substrates, on the other hand, were placed downstream (1–5 cm) from the alumina crucible. The advantage of this setup is as follows: by varying the carrier gas flow rate and the pressure inside the reactor, it is possible to have different zinc vapor and oxygen gas partial pressures along the small diameter tube, starting from highest zinc vapor concentration at the closed/hot end to highest oxygen pressure at the open/cold end. Therefore, with this setup it was fairly easy to arrive at the optimal parameters for the ideal nanowire growth conditions. After loading the source materials and the silicon substrates into the inner tube, the complete system was evacuated to 1 mbar under a 10 sccm flow of carrier gas (1 vol% O_2 and 99 vol% Ar) and was kept under continuous evacuation for about 45 min in order to make the reaction atmosphere free from any polluting or unwanted gas species. Next, the reactor was introduced into the tube furnace which was already heated to 945 °C. Immediately, after insertion of the tube, the temperature of the furnace was dropped rapidly down to 910 °C. The reactor was then kept at this temperature for about 10 min and subsequently moved out of the furnace and allowed to cool down to room temperature. Finally, the substrates were taken out of the reactor and a dense white layer of as-grown ZnO nanowires were observed on most of the substrates.

Characterization: As-prepared nanowires were analyzed using a Philips X'PERT X-ray diffractometer with Cu-$K\alpha$ target which was operated at 45 kV, 40 mA. The morphology and the chemical analysis (EDX) of the nanowires were carried out with a Leo 1530 Gemini scanning electron microscope (SEM). Transmission electron microscopy (TEM) was performed using FEI Titan 80–300.

Electrolyte Preparation: The composite solid polymer electrolyte (CSPE) used in this work is composed of a synthetic polymer (poly(vinyl alcohol) (PVA), average M_w = 13–23 kDa, 98% hydrolyzed, Sigma-Aldrich), a plasticizer (propylene carbonate (PC), anhydrous, 99.7%, Sigma-Aldrich), a supporting electrolyte/salt (lithium perchlorate, $LiClO_4$, anhydrous, 98% Alfa Aesar) and a solvent (dimethyl sulfoxide, DMSO, anhydrous 99.9% Sigma-Aldrich), all of these were used as received and without any further purification. In order to prepare the CSPE, first PVA was added to DMSO and the solution was then stirred and heated continuously at 80–100 °C for several hours until the mixture became a homogeneous sol. Next, lithium perchlorate was dissolved in PC and added to the PVA solution. The complete mixture was then stirred at room temperature for about 12–24 h to obtain a completely single phase, clear and homogeneous solution (liquid electrolyte) which was then used to print the composite solid polymer electrolyte. For the optimum performance of the polymer-gel electrolyte the PVA: PC: $LiClO_4$ ratio was kept at 30:63:7. In order to ensure easy printability, the weight of DMSO was usually taken 5–6 times larger compared to the total weight of all the other components together.

Device Fabrication: In order to build the nanowire based EG FET devices, the as-grown ZnO nanowires were transferred from the growth substrate (donor) to the oxygen plasma-cleaned receiver (Si/SiO_2wafer) substrate. Several individual ZnO nanowires were then selected and their positions are marked or defined using SEM. Electron beam lithography (EBL) was used to pattern the passive structures onto the selected nanowires. Using RF magnetron sputtering, tin doped indium oxide (ITO) with approximate thickness of 30 nm was deposited onto the nanowires in order to ensure ohmic contacts with the ZnO nanowires. This was followed by the lift-off of the e-beam resist (PMMA, A4.5, 950 K, Allresist GmbH). In this way, the contact electrodes, such as the source, the drain and the in-plane gate electrodes were constructed; the distance between the source and the drain electrode was usually kept around 1–2 µm whereas the distance of the gate electrode from the nanowire channel was maintained approximately 10 µm. The printing of the electrolyte was performed with a commercially available Dimatix DMP 2831 ink-jet printer having piezoelectric nozzles with nozzle diameter of 21.5 µm. The electrolyte was always printed in a way to cover the nanowire channel completely and the in-plane gate electrode partially.

Electrical Measurements: The transfer and the current-voltage output characteristics of the transistors were measured with a precision semiconductor parameter analyzer (Agilent 4156C) under ambient conditions at room temperature. The transient measurements were performed using a semiconductor characterization system (Keithley 4200-SCS) equipped with pulse measure units (PMU) and low current modules (RPM). In all mentioned electrical measurements the devices were connected to electronic systems through a grounded probe station (SÜSS MicroTec PE6).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] L. Wang, M.-H. Yoon, A. Facchetti, T. J. Marks, *Adv. Mater.* **2007**, *19*, 3252.
[2] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, H. Hosono, *Science* **2003**, *300*, 1269.
[3] M. Yan, M. Lane, C. R. Kannewurf, R. P. H. Chang, *Appl. Phys. Lett.* **2001**, *78*, 2342.
[4] P. Barquinha, L. Pereira, G. Gonćalves, R. Martins, E. Fortunato, *J. Electrochem. Soc.* **2009**, *156*, H161.
[5] L. Wang, M.-H. Yoon, G. Lu, Y. Yang, A. Facchetti, T. J. Marks, *Nat. Mater.* **2006**, *5*, 893.
[6] K. Baler, *REU Research Accomplishments* **2007**, 42.
[7] H.-Y. Chen, H.-C. Su, C.-H. Chen, K.-L. Liu, C.-M. Tsai, S.-J. Yen, T.-R. Yew, *J. Mater. Chem.* **2011**, *21*, 5745.
[8] S. Ju, A. Facchetti, Y. Xuan, J. Liu, F. Ishikawa, P. Ye, C. Zhou, T. J. Marks, D. B. Janes, *Nat. Nanotechnol.* **2007**, *2*, 378.

[9] J. Park, Y. Kim, G.-T. Kim, J. S. Ha, *Adv. Funct. Mater.* **2011**, *21*, 4159.
[10] W. F. Zhang, Z. B. He, G. D. Yuan, J. S. Jie, L. B. Luo, X. J. Zhang, Z. H. Chen, C. S. Lee, W. J. Zhang, S. T. Lee, *Appl. Phys. Lett.* **2009**, *94*, 123103.
[11] S. Ju, J. Li, J. Liu, P.-C. Chen, Y.-G. Ha, F. Ishikawa, H. Chang, C. Zhou, A. Facchetti, D. B. Janes, T. J. Marks, *Nano Lett.* **2008**, *8*, 997.
[12] Z. Fan, J. C. Ho, T. Takahashi, R. Yerushalmi, K. Takei, A. C. Ford, Y.-L. Chueh, A. Javey, *Adv. Mater.* **2009**, *21*, 3730.
[13] K. Keem, D.-Y. Jeong, S. Kim, M.-S. Lee, I.-S. Yeo, U.-I. Chung, J.-T. Moon, *Nano Lett.* **2006**, *6*, 1454.
[14] D.-I. Suh, S.-Y. Lee, J.-H. Hyung, T.-H. Kim, S.-K. Lee, *J. Phys. Chem. C* **2008**, *112*, 1276.
[15] G. Adamopoulos, S. Thomas, P. H. Wöbkenberg, D. D. C. Bradley, M. A. McLachlan, T. D. Anthopoulos, *Adv. Mater.* **2011**, *23*, 1894.
[16] L. Liao, H. J. Fan, B. Yan, Z. Zhang, L. L. Chen, B. S. Li, G. Z. Xing, Z. X. Shen, T. Wu, X. W. Sun, J. Wang, T. Yu, *ACS Nano* **2009**, *3*, 700.
[17] D.-I. Suh, S.-Y. Lee, J.-H. Hyung, T.-H. Kim, S.-K. Lee, *J. Phys. Chem. C* **2008**, *112*, 1276.
[18] K. A. Cimatu, S. M. Mahurin, K. A. Meyer, R. W. Shaw, *J. Phys. Chem. C* **2012**, *116*, 10405.
[19] P. Jood, R. J. Mehta, Y. Zhang, G. Peleckis, X. Wang, R. W. Siegel, T. Borca-Tasciuc, S. X. Dou, G. Ramanath, *Nano Lett.* **2011**, *11*, 4337.
[20] C. Lu, L. Qi, J. Yang, L. Tang, D. Zhang, J. Ma, *Chem. Commun.* **2006**, 3551.
[21] P. Chen, G. Shen, H. Chen, Y. Ha, C. Wu, K. S. Sukcharoenchoke, Y. Fu, J. Liu, A. Facchetti, T. J. Marks, M. E. Thompson, C. Zhou, *ACS Nano* **2009**, *3*, 3383.
[22] M. C. Mcalpine, R. S. Friedman, C. M. Lieber, *Proc. IEEE* **2005**, *93*, 1357.
[23] Y. Sun, H.-S. Kim, E. Menard, S. Kim, I. Adesida, J. A. Rogers, *Small.* **2006**, *2*, 1330.
[24] M. C. McAlpine, H. Ahmad, D. Wang, J. R. Heath, *Nat. Mater.* **2007**, *6*, 379.
[25] H. T. Ng, J. Han, T. Yamada, P. Nguyen, Y. P. Chen, M. Meyyappan, *Nano Lett.* **2004**, *4*, 1247.
[26] T.-H. Moon, M.-C. Jeong, B.-Y. Oh, M.-H. Ham, M.-H. Jeun, W.-Y. Lee, J.-M. Myoung, *Nanotechnology* **2006**, *17*, 2116.
[27] D. Yeom, K. Keem, J. Kang, D.-Y. Jeong, C. Yoon, D. Kim, S. Kim, *Nanotechnology* **2008**, *19*, 265202.
[28] S. A. DiBenedetto, A. Facchetti, M. A. Ratner, T. J. Marks, *Adv. Mater.* **2009**, *21*, 1407.
[29] S. M. C. Vieira, G.-W. Hsieh, H. E. Unalan, S. Dag, G. A. J. Amaratunga, W. I. Milne, *Appl. Phys. Lett.* **2011**, *98*, 102106.
[30] D. Kälblein, R. T. Weitz, H. J. Böttcher, F. Ante, U. Zschieschang, K. Kern, H. Klauk, *Nano Lett.* **2011**, *11*, 5309.
[31] S. Ju, K. Lee, D. B. Janes, M.-H. Yoon, A. Facchetti, T. J. Marks, *Nano Lett.* **2005**, *5*, 2281.
[32] S. Ju, D. B. Janes, G. Lu, A. Facchetti, T. J. Marks, *Appl. Phys. Lett.* **2006**, *89*, 193506.
[33] L. Wang, M.-H. Yoon, G. Lu, Y. Yang, A. Facchetti, T. J. Marks, *Nat. Mater.* **2006**, *5*, 893.
[34] S. Ju, F. Ishikawa, P. Chen, H.-K. Chang, C. Zhou, Y. Ha, J. Liu, A. Facchetti, T. J. Marks, D. B. Janes, *Appl. Phys. Lett.* **2008**, *92*, 222105.
[35] S. Thiemann, S. Sachnov, S. Porscha, P. Wasserscheid, J. Zaumseil, *J. Phys. Chem. C* **2012**, *116*, 13536.
[36] S. Bai, W. Wu, Y. Qin, N. Cui, D. J. Bayerl, X. Wang, *Adv. Funct. Mater.* **2011**, *21*, 4464.
[37] M. Law, L. E. Greene, J. C. Johnson, R. Saykally, P. Yang, *Nat. Mater.* **2005**, *4*, 455.
[38] R. S. Wagner, W. C. Ellis, *Appl. Phys. Lett.* **1964**, *4*, 89.
[39] M. J. Hÿtch, E. Snoeck, R. Kilaas, *Ultramicroscopy* **1998**, *74*, 131.
[40] S. Dasgupta, G. Stoesser, N. Schweikert, R. Hahn, S. Dehm, R. Kruk, H. Hahn, *Adv. Funct. Mater.* **2012**, DOI: 10.1002/adfm.201200951.
[41] K. K. Sze, S. M. Ng, *Physics of Semiconductor Devices* John Wiley & Sons, Hoboken, New York **2007**.
[42] T. Uemura, R. Hirahara, Y. Tominari, S. Ono, S. Seki, J. Takeya, *Appl. Phys. Lett.* **2008**, *93*, 263305.
[43] S. Ono, N. Minder, Z. Chen, A. Facchetti, A. F. Morpurgo, *Appl. Phys. Lett.* **2010**, *97*, 143307.
[44] H. Shimotani, H. Asanuma, A. Tsukazaki, A. Ohtomo, M. Kawasaki, Y. Iwasa, *Appl. Phys. Lett.* **2007**, *91*, 082106.
[45] M. I. Dzhavaichidze, P. G. Kornyshev, A. A. Liebsch, A. Urbakh, *Electrochim. Acta* **1991**, *36*, 1835.
[46] P. Dzhavakhidze, A. Kornyshev, A. Liebsch, M. Urbakh, *Phys. Rev. B.* **1992**, *45*, 9339.
[47] K. Izutsu, *Electrochemistry Nonaqueous Solutions*, Vol. *5*, Wiley VCH, Weinheim **2002**.
[48] R. Ponce Ortiz, A. Facchetti, T. J. Marks, *Chem. Rev.* **2010**, *110*, 205.
[49] L. Herlogsson, Y.-Y. Noh, N. Zhao, X. Crispin, H. Sirringhaus, M. Berggren, *Adv. Mater.* **2008**, *20*, 4708.
[50] R. Misra, M. McCarthy, A. F. Hebard, *Appl. Phys. Lett.* **2007**, *90*, 052905.
[51] J. H. Cho, J. Lee, Y. Xia, B. Kim, Y. He, M. J. Renn, T. P. Lodge, C. D. Frisbie, *Nat. Mater.* **2008**, *7*, 900.
[52] L. Herlogsson, M. Cölle, S. Tierney, X. Crispin, M. Berggren, *Adv. Mater.* **2010**, *22*, 72.
[53] J. Lee, L. G. Kaake, J. H. Cho, X.-Y. Zhu, T. P. Lodge, C. D. Frisbie, *J. Phys. Chem. C* **2009**, *113*, 8972.
[54] J. Lee, M. J. Panzer, Y. He, T. P. Lodge, C. D. Frisbie, *J. Am. Chem. Soc.* **2007**, *129*, 4532.
[55] J. Liu, L. Herlogsson, A. Sawatdee, P. Favia, M. Sandberg, X. Crispin, I. Engquist, M. Berggren, *Appl. Phys. Lett.* **2010**, *97*, 103303.